IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:

Ari PEKKARINEN et al	:	Confirmation No. **6761**
Serial No: **10/582,833**	:	Examiner: **Feifei Yeung Lopez**
Filed: **June 14, 2006**	:	Group Art Unit: **2826**

For: **METHOD AND ARRANGEMENT FOR SHIELDING AN ELEMENT AGAINST ELECTRASTATIC INTERFERENCE**

Mail Stop Appeal Briefs-Patents
Commission for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF FOR APPELLANT (37 C.F.R. § 41.37)

Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on April 8, 2010. This is an appeal from the final Office Action mailed December 8, 2009 rejecting claims 1-20.

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Briefs-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

6.29.10

Cathy Sturmer — Date

07/02/2010 MBELETE1 00000036 10582833
02 FC:1402 540.00 OP

I. REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is Nokia Corporation, a corporation organized under the laws of Finland.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c)(1)(ii))

There are no related appeals or interferences.

III. STATUS OF CLAIMS (37 C.F.R. § 41.37(c)(1)(iii))

Claims 1-20 are pending in this application. Claim 1-20 are rejected, and the rejection of claims 1-20 is being appealed.

IV. STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

No amendment was filed after the final rejection, and therefore all amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

Independent claim 1 is directed to a semiconductor component that includes a semiconductor element. *See* specification page 3, lines 22-23; page 5, lines 12-16; page 6, lines 29-30; Figure 1 (102); Figure 2 (202). The semiconductor element is encased by a cover. *See* specification page 5, lines 20-22; page 6, lines 33-34; Figure 1 (104); Figure 2 (204). The cover element has an integrated electroconductive metal element. *See* Figure 1 (105); specification page 6, lines 32-34; Figure 2 (205). The integrated electroconductive metal element includes at least one outlet. *See* specification page 6, lines 1-2; page 7, lines 7-8; Figure 1 (106); Figure 2 (206). The at least one outlet is configured to constantly connect the electroconductive metal element to ground in order to shield the semiconductor element against electrostatic pulses. *See* specification page 6, lines 1-4; page 7, lines 8-12; Figure 1 (106).

Independent claim 8 is directed to a method for shielding a semiconductor element against electrostatic pulses that includes integrating the semiconductor element in a semiconductor component. *See* specification page 3, lines 22-23; page 5, lines 12-16; page 6, lines 29-30; Figure 1 (102); Figure 2 (202). The method also includes covering the semiconductor element with a cover element. *See* specification page 5, lines 20-22; page 6, lines

33-34; Figure 1 (104); Figure 2 (204). The method further includes integrating an electroconductive metal element within the cover element of the semiconductor component. *See* Figure 1 (105); specification page 6, lines 32-34; Figure 2 (205). The method also includes providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to constantly connect the electroconductive metal element to ground. *See* specification page 6, lines 1-4; page 7, lines 7-12; Figure 1 (106); Figure 2 (206).

Independent claim 15 is directed to an arrangement including a mounting tray and at least one semiconductor component. *See* specification page 3, lines 34-35. The at least one semiconductor component includes a semiconductor element. *See* specification page 3, lines 22-23; page 5, lines 12-16; page 6, lines 29-30; Figure 1 (102); Figure 2 (202). The semiconductor element is encased by a cover element. *See* specification page 5, lines 20-22; page 6, lines 33-34; Figure 1 (104); Figure 2 (204). The cover element has an integrated electroconductive metal element. *See* Figure 1 (105); specification page 6, lines 32-34; Figure 2 (205). The electroconductive metal element is provided with at least one outlet that is constantly grounded to a ground plane of the mounting tray. *See* specification page 6, lines 1-4; page 7, lines 7-12; Figure 1 (106); Figure 2 (206).

Independent claim 16 is directed to an apparatus for shielding a semiconductor element against electrostatic pulses. *See* specification page 3, lines 22-23. The apparatus includes means for covering the semiconductor element in a semiconductor component having an integrated electroconductive metal element. *See* specification page 5, lines 20-22; page 6, lines 33-34; Figure 1 (104); Figure 2 (204). The apparatus also includes means for providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to constantly connect the electroconductive metal element to ground. *See* specification page 6, lines 1-4; page 7, lines 7-12; Figure 1 (106); Figure 2 (206).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

Claims 1-20 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 1-20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 4-5, 8, 11-12, 15-16 and 19-20 are rejected under 35 U.S.C. § 102(b) as anticipated by *Hong et al.* (U.S. Patent No. 5,889,308).

Claims 1, 2, 4-9, 11-14, 16-17 and 19-20 are rejected under 35 U.S.C. §102(b) as anticipated by *Sherwood et al.* (U.S. Patent No. 4,303,960).

Claims 1, 3, 8, 10, 16 and 18 are rejected under 35 U.S.C. § 102(b) as anticipated by *Wu et al.* (U.S. Patent No. 6,175,394).

VII. ARGUMENT (37 C.F.R. § 41.37(c)(1)(vii))

Rejection under 35 U.S.C. § 112, first paragraph, for written description requirement

Claim 1

The Office asserts on page 2 of the final Office Action of December 8, 2009 that the term "constantly" is not used in the specification for the present application, and that the device accordingly to an exemplary embodiment of the invention requires a certain amount of minimum voltage or current for the electroconductive element to conduct current to ground. Appellant acknowledges that the term "constantly" is not explicitly mentioned in the description. However, the subject matter of the claim need not be described literally, i.e. using the same terms, in order for the disclosure to satisfy the description requirement. *See* MPEP § 2163.02. It is evident from Figures 1-3 and specification that the outlet, e.g. 106 in Figure 1, constantly connects the electroconductive metal element to ground. *See* specification page 6, lines 1-6. This section of the specification specifically states that electrostatic pulses coming to the electroconductive element are conducted to the ground plane. *See* specification page 6, lines 3-4. This applies to all embodiments described in the specification. *See* specification page 7, lines 7-12; page 8, lines 22-26. Appellant respectfully submits that circuit diagrams are an established way of describing electrical connections, and the skilled person will interpret a diagram as describing a constant connection, unless it is specifically indicated otherwise in the diagram. As mentioned above, the specification specifically states that electrostatic pulses are conducted to the ground plane, and does not discuss any limitation as to the requirements for an electrostatic pulse to be conducted to the ground plane. Accordingly, the skilled person would have no difficulty in finding support from and understanding that drawings of the present application unambiguously describe a constant connection. For at least the reasons discussed above, appellant respectfully submits that claim 1 is supported by the specification.

Claims 8 and 15-16

Independent claims 8 and 15-16 also recite the term "constantly," and are rejected for the same reason as claim 1. For at least the reasons discussed above with respect to claim 1, appellant respectfully submits that claims 8 and 15-16 are supported by the specification.

Claims 2-7, 9-14 and 17-20

Claims 2-7, 9-14 and 17-20 ultimately depend from an independent claim, and therefore are supported by the specification for at least the reasons discussed above with respect to the independent claims from which they depend from.

Rejection under 35 U.S.C. § 112, second paragraph, for indefinitiveness

Claim 1

The Office asserts on page 3 of the final Office Action of December 8, 2009 that it is not clear what appellant means by the phrase "constantly connect the electroconductive element to ground" recited in claim 1. Appellant respectfully submits that contact potentials between dissimilar materials exist and are present in many electrical circuits and connections in some form. However, the skilled person would consider an electrical connection to be constant, i.e. always-on, unless such contact potentials are strong enough to affect functioning of the electrical connection in a noticeable way. Thus even if an electrical connection is described as "configured to constantly connect," the skilled person will understand that small contact potentials may be present. The Office asserts that appellant interprets that there is a constant current flow from the electroconductive metal element to ground, and that it is unclear where and how the constant electrostatic current comes from. However, appellant respectfully submits that this interpretation is not required by the claims. Instead, the phrase "configured to constantly connect" means a capability to conduct is constantly present. The limitation does not require a constant current flow, but rather that the outlet is configured to constantly connect the electroconductive metal element to ground. The specification specifically states that electrostatic pulses coming to the electroconductive element are conducted to the ground plane. *See* specification page 6, lines 3-4. Therefore, when an electrostatic pulse is introduced to the electroconductive element it is conducted to the ground plane, because the outlet is configured to constantly connect the electroconductive metal element to ground. Therefore the limitation of "configured to constantly connect" is supported and clear, it means that a capability to conduct is constantly present, and the phrase cannot be taken to mean that current is constantly flowing. Accordingly, for at least the reasons discussed above, appellant respectfully submits that claim 1 is definite.

Claims 8 and 15-16

Independent claims 8 and 15-16 also recite the term "constantly connect the electroconductive element to ground," and are rejected for the same reason as claim 1. For at least the reasons discussed above with respect to claim 1, appellant respectfully submits that claims 8 and 15-16 are definite.

Claims 2-7, 9-14 and 17-20

Claims 2-7, 9-14 and 17-20 ultimately depend from an independent claim, and therefore are definite for at least the reasons discussed above with respect to the independent claims from which they depend from.

Rejection under 35 U.S.C. § 102(b) in view of U.S. Patent No. 5,889,308

Claim 1

Appellant respectfully submits that claim 1 is not disclosed or suggested by *Hong*, because *Hong* fails to disclose or suggest all of the limitations recited in claim 1. *Hong* at least fails to disclose or suggest at least one outlet is configured to constantly connect the electroconductive metal element to ground, as recited in claim 1. In contrast to claim 1, *Hong* is directed to a shielding solution based on a varistortype (non-ohmic) electrical connection which turns into a conducting state only when a certain threshold voltage is exceeded. *Hong* teaches an intermittent connection which is carried out using a non-ohmic device, such as a varistor. *Hong* teaches a non-ohmic varistor-type electrical connection in which a non-ohmic material acts as an insulator below the specific voltage, and acts as an excellent conductor in voltage more than the specific voltage. *See Hong* column 3, lines 1-8. Therefore, *Hong's* electrical connection is intermittent so that sometimes it is on (conducting state) and sometimes it is off (insulator state). Instead, the varistor-type electrical connection only acts as a connection when a voltage more than the specific voltage is applied. Accordingly, *Hong* fails to disclose or suggest an outline configured to constantly connect an electroconductive metal element to ground, as recited in claim 1. For at least this reason, claim 1 is not disclosed or suggested by *Hong*.

Claims 8 and 15-16

Independent claims 8 and 15-16 contain limitations similar to those recited in claim 1. Therefore, for at least the reasons discussed above with respect to claim 1, claims 8 and 15-16 are not disclosed or suggested by *Hong*.

Claims 4-5, 11-12 and 19-20

Claims 4-5, 11-12 and 19-20 ultimately depend from an independent claim, and therefore are not disclosed or suggested by *Hong* for at least the reasons discussed above with respect to the independent claims from which they depend from.

Rejection under 35 U.S.C. §102(b) in view of U.S. Patent No. 4,303,960

Claim 1

Appellant respectfully submits that claim 1 is not disclosed or suggested by *Sherwood*, because *Sherwood* fails to disclose or suggest all of the limitations recited in claim 1. *Sherwood* at least fails to disclose or suggest at least one outlet is configured to constantly connect the electroconductive metal element to ground, as recited in claim 1. In contrast to claim 1, *Sherwood* is directed to an intermittent connection which is carried out using dielectric Mylar sheet. According to *Sherwood* when an electrostatic charge stored by subscriber's body exceeds the barrier potential established by the Mylar faceplate, it is discharged from his finger into the conductive surface (75) on the back of the face plate, and through pad (65), printed wire (63), a line (63') on circuit board, a wire of cable (24) and line (14) to ground for protecting the microprocessor. *See Sherwood* column 4, lines 57-65. Therefore, the conductive surface acts as an excellent conductor in voltage more than the specific voltage and acts as an insulator below the specific voltage. Accordingly, *Sherwood* does not teach that an outlet is configured to constantly connect the electroconductive metal element to ground, as recited in claim 1. Instead, *Sherwood* teaches that the cable (24) is attached to the processor (10) and the plug (88) in the control unit for electrically connecting. *See Sherwood* column 4, lines 46-49. The cable (24) can be unplugged from the plug (88). Therefore, *Sherwood* does not teach that an outlet is configured to constantly connect the electroconductive metal element to ground, as recited in claim 1. For at least the reasons discussed above, claim 1 is not disclosed or suggested by *Sherwood*.

Claims 8 and 15-16

Independent claims 8 and 15-16 contain limitations similar to those recited in claim 1. Therefore, for at least the reasons discussed above with respect to claim 1, claims 8 and 15-16 are not disclosed or suggested by *Sherwood.*

Claims 2, 4-7, 9, 11-14, 17 and 19-20

Claims 2, 4-7, 9, 11-14, 17 and 19-20 ultimately depend from an independent claim, and therefore are not disclosed or suggested by *Sherwood* for at least the reasons discussed above with respect to the independent claims from which they depend from.

Rejection under 35 U.S.C. § 102(b) in view of U.S. Patent No. 6,175,394

Claim 1

Appellant respectfully submits that claim 1 is not disclosed or suggested by *Wu*, because *Wu* fails to disclose or suggest all of the limitations recited in claim 1. *Wu* at least fails to disclose or suggest at least one outlet is configured to constantly connect the electroconductive metal element to ground, as recited in claim 1. *Wu* teaches an intermittent connection which is carried out using a guard ring (130). In *Wu*, (col. 8, lines 2-4) for typical assembly and test operations, the guard ring (130) is held at a fixed potential such as ground. *See Wu* column 8, lines 2-4. *Wu* does not teach that for normal operation the guard ring (130) is held at a fixed potential such as ground. Therefore, *Wu* does not disclose that for all operations (including normal, standby, assembly, test, etc. operations) the guard ring (130) is held at a fixed potential such as ground. Accordingly, the guard ring (130) is not configured to constantly connect to ground, since during normal operation the guard ring (130) is not held at ground. Therefore, *Wu* does not disclose that an outlet is configured to constantly connect the electroconductive metal element to ground, as recited in claim 1. For at least this reason, claim 1 is not disclosed or suggested by *Wu.*

Claims 8 and 16

Independent claims 8 and 16 contain limitations similar to those recited in claim 1. Therefore, for at least the reasons discussed above with respect to claim 1, claims 8 and 16 are not disclosed or suggested by *Wu*.

Claims 3, 10 and 18

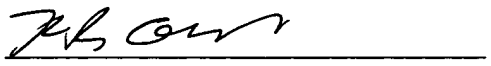
Claims 3, 10 and 18 ultimately depend from an independent claim, and therefore are not disclosed or suggested by *Wu* for at least the reasons discussed above with respect to the independent claims from which they depend from.

Conclusion

For the reasons discussed above, applicant respectfully submits that the rejections of the final Office Action have been shown to be inapplicable, and respectfully requests that the Board reverse the rejections of pending claims 1-20. If any additional fee is required for submission of this Appeal Brief, the Commissioner is hereby authorized to charge Deposit Account No. 23-0442.

Respectfully submitted,

Date: 29 June 2010



Keith R. Obert
Attorney for the Appellant
Registration No. 58,051

WARE, FRESSOLA, VAN DER SLUYS
& ADOLPHSON LLP
755 Main Street, P.O. Box 224
Monroe, CT 06468
Telephone: (203) 261-1234
Facsimile: (203) 261-5676
USPTO Customer No. 004955

CLAIMS APPENDIX

1. A semiconductor component, comprising a semiconductor element encased by a cover element having an integrated electroconductive metal element comprising at least one outlet, wherein the at least one outlet is configured to constantly connect the electroconductive metal element to ground in order to shield the semiconductor element against electrostatic pulses.

2. A semiconductor component according to claim 1, wherein in structure, the electroconductive metal element is a planar sheet.

3. A semiconductor component according to claim 1, wherein the electroconductive metal element is a thin loop structure.

4. A semiconductor component according to claim 1, wherein the electroconductive metal element forms a permanent, integrated part of the semiconductor component.

5. A semiconductor component according to claim 1, wherein the electroconductive metal element is placed underneath the cover element of the semiconductor component, inside said cover element.

6. A semiconductor component according to claim 1, wherein the electroconductive metal element is attached to the cover element of the semiconductor component, outside said cover element.

7. A semiconductor component according to claim 1, wherein the electroconductive metal element is induced in the cover element of the semiconductor component either chemically or electrochemically.

8. A method for shielding a semiconductor element against electrostatic pulses, comprising: integrating the semiconductor element in a semiconductor component, covering the semiconductor element with a cover element, integrating an electroconductive metal element within the cover element of the semiconductor component and providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to constantly connect the electroconductive metal element to ground.

9. A method according to claim 8, wherein in the semiconductor component, there is integrated an electroconductive, planar metal element.

10. A method according to claim 8, wherein in the semiconductor component, there is integrated an electroconductive, loop-shaped metal element.

11. A method according to claim 8, wherein the electroconductive metal element is integrated as a permanent part of the semiconductor component.

12. A method according to claim 11, wherein the electroconductive metal element is placed underneath the cover element of the semiconductor component, inside said cover element.

13. A method according to claim 11, wherein the electroconductive metal element is attached to the cover element of the semiconductor component, outside said cover element.

14. A method according to claim 8, wherein the electroconductive metal element is induced in the cover element of the semiconductor component either chemically or electrochemically.

15. An arrangement including a mounting tray and at least one semiconductor component, wherein said at least one semiconductor component comprises a semiconductor element encased by a cover element having an integrated electroconductive metal element, where the electroconductive metal element is provided with at least one outlet that is constantly grounded to a ground plane of the mounting tray.

16. Apparatus for shielding a semiconductor element against electrostatic pulses, comprising:

means for covering the semiconductor element in a semiconductor component having an integrated electroconductive metal element; and

means for providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to constantly connect the electroconductive metal element to ground.

17. The apparatus of claim 16, wherein in the semiconductor component, there is integrated an electroconductive, planar metal element.

18. The apparatus of claim 16, wherein in the semiconductor component, there is integrated an electroconductive, loop-shaped metal element.

19. The apparatus of claim 16, wherein the electroconductive metal element is integrated as a permanent part of the semiconductor component.

20. The apparatus of claim 16, wherein the electroconductive metal element is integrated underneath the means for covering the semiconductor component, inside said cover element.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.